Amendments of the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Please amend claims 14, 16 – 24, 26, 27, 33, 41 and 42, as follows:

Listing of claims.

1. (Original) A digital processing system comprising:

a first semiconductor device having a plurality of computation nodes;

a second semiconductor device having a microprocessor-based node adapted to function as a system controller and a plurality of computation nodes; and

a bus for inter-connecting said first semiconductor device to said second semiconductor device in a ring topology whereby the microprocessor-based node allocates a plurality of operations among said computation nodes of said first and second semiconductor devices over said inter-connecting bus and receives the results of said operations over said inter-connecting bus.

2. (Original) The digital processing system of claim 1 wherein said computation nodes on said first and second semiconductor devices include at least one of the following node types: an arithmetic node, a bit manipulation node, a reduced instruction set processing node and a finite state machine node.

3. (Original) The digital processing system of claim 1 wherein the digital system includes a plurality of nodes each of which can perform at least one type of operation and wherein said microprocessor node allocates functions temporally and spatially among the nodes of said first and second semiconductor devices.

4. (Original) The digital processing system of claim 1 further comprising:

a remote processor; and a second bus for interfacing said first and second semiconductor device to said remote processor.

5. (Original) The digital processing system of claim 4 further comprising:

a real-time data source; and

a third bus for interfacing said first and second semiconductor device to said real-time data generator.

6. (Original) The inter-connecting bus of the digital processing system of claim 1 further comprising:

a plurality of logic elements, each closely proximate to a corresponding output pad of said first semiconductor device, for sending data and control signals;

a plurality of logic elements, each closely proximate to a corresponding input pad of said second semiconductor device, for receiving said data and control signals;

and means for synchronously transferring data and control logic by clocking the logic elements of said first and second semiconductor devices.

7. (Original) The digital processing system of claim 6 further comprising:

a first core logic clock signal provided to each of said nodes of said first semiconductor device;

a second core logic clock signal provided to each of said nodes of said second semiconductor device, said first and second core logic clocks having substantially the same frequency and phase;

a first bus clock for clocking said logic elements of said first semiconductor device at a selected rate where said first bus clock is derived from said first core logic clock;

a second bus clock for clocking said logic elements of said second semiconductor device at said selected rate where said second bus clock is derived from said second core logic clock; and

a synchronizing signal generated by said first semiconductor device.

8. (Original) The digital processing system of claim 1 further comprising:

a first core logic clock signal provided to each of said nodes of said first semiconductor device;

a second core logic clock signal provided to each of said nodes of said second semiconductor device, said first and second core logic clocks having substantially the same frequency and phase; and

means for synchronizing the transfer for data and control signals from said first semiconductor device to said second semiconductor device, said synchronizing means derived from said first core logic clock signal.

9. (Original) The synchronizing means of claim 8 further comprising:

a first bus clock for clocking said logic elements of said first semiconductor device at a selected rate where said first bus clock is derived from said first core logic clock;

a second bus clock for clocking said logic elements of said second semiconductor device at said selected rate where said second bus clock is derived from said second core logic clock; and

a signal, generated by said first semiconductor device, for indicating valid data and control signals to said second semiconductor device.

10. (Original) The digital processing system of claim 1 wherein said first and second semiconductor devices are coupled in a ring with said inter-connecting bus coupling an output port of said first semiconductor device to an input port of said second semiconductor device and further coupling an output port of said second semiconductor device to an input port of said first semiconductor device.

11. (Original) The digital processing system of claim 1 wherein said microprocessor-based node determines whether a packet received on said second bus is addressed to a node on either said first or second semiconductor device.

12. (Original) The digital processing system of claim 11 wherein said microprocessor-based node passes said packet to one of said plurality of computation nodes on said first semiconductor device if said packet is addressed to a node on said first semiconductor device or transferring said packet to one of said plurality of computation nodes on said second semiconductor device if said packet is addressed to a node on said second semiconductor device where said packet is transferred on said inter-connecting bus.

13. (Original) The digital processing system of claim 11 wherein said packet includes a device identification field.

14. (Currently amended) A digital processing system comprising:

a plurality of adaptive computing engines each having a plurality of computation nodes;

said adaptive computing engines coupled to each other by in a ring topology ~~by a~~ bus that couples a first adaptive computing engine to a second adaptive computing engine, couples said second adaptive computing engine to a third adaptive computing engine and couples said third adaptive computing engine to said first adaptive computing engine, said bus adapted for passing packets between said computation nodes by passing them around said ring topology bus;

one of said adaptive computing engines having a kernel node, said kernel node adapted for determining whether a packet is addressed ~~intended~~ for one of said computation nodes in one of said adaptive computing engines and for discarding packets ~~intended for~~ addressed to computational nodes that are not part of said digital processing system.

15. (Original) The digital processing system of claim 14, wherein each of said adaptive computing engines includes a device identification number and said packet includes a device identification field.

16. (Currently amended) The digital processing system of claim 15, wherein each adaptive computing engine includes an output port coupled to an input port of the next adjacent adaptive computing engine in said ring topology bus.

17. (Currently amended) The digital processing system of claim 16, wherein said ring topology bus comprises more than two ~~, three or four~~ adaptive computing engines.

18. (Currently amended) The digital processing system of claim [[14]] 16 wherein at least one of said output ~~port~~ ports comprises a plurality of D type flip flops coupled to a corresponding plurality of D type flip flops at said input port.

19. (Currently amended) A method for transferring information from one adaptive computing engine having a plurality of computational nodes to another adaptive computing engine having a second plurality of computational nodes, each adaptive computing engine having an input port and an output port, said adaptive computing engines being coupled to each other through a ring topology bus, said method comprising the steps of:

~~Generating~~ generating a common clock signal routed to at least two adaptive computing engines;

~~Requesting~~ requesting to transfer information from a first ~~one~~ adaptive computing engine to ~~another~~ a second adaptive computing engine via said ring topology bus;

~~Offering~~ offering to receive said information;

~~Transferring~~ transferring said information from a D type flip flop associated with an output port of a first adaptive computing engine ~~said output port~~ to a D type flip flop associated with an input port of a second adaptive computing engine via said ring topology bus; ~~said input port;~~

~~Controlling~~ controlling the transfer of said information from said D type flip flop associated with said output port of said first adaptive computing engine with a first clock derived from said common clock signal;

~~Controlling~~ controlling the receipt of said information by said D type flip flop associated with said input port of said second adaptive computing engine with a second clock derived from said common clock signal; and

~~Generating~~ generating a signal to define a time period window during which the